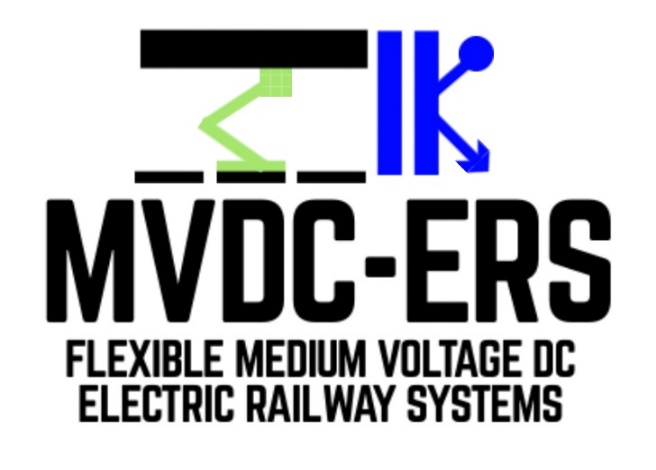


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# Introduction and executive summary

The present report constitutes deliverable D2.2, a document produced in the framework of WP2 “Medium Voltage (MV) DC transformers for railway traction”, Task 2.2 “Development of a simulation model for DC based power transformers” and Task 2.3 “Experimental verification on a small-scale prototype”.

The objectives of WP2 is to undertake a comparative evaluation of topologies for the medium voltage DC transformers, to define the optimal topology for railway traction applications including evaluation of the performance of the converter and to develop a software model for the prediction of static and dynamic performance of the DC transformer, as well as an experimental prototype.

Hence this report is a summary of this work package, focused on the design and implementation of the DC transformer, it offers a critical analysis and comparison of the chosen topologies in D2.1. In D2.1 the conventional railway traction systems were compared with new traction systems suitable for the MVDC railway electrification concept. Since a review about the impact of new wide-band-gap (WBG) semiconductor technologies was already included in D2.1, here will not be treated in detail again, only some losses evaluation method will be presented, and power density improvements, as a result of their impact. This report however, includes the mathematical model of two converter topologies along with the design equations of their controllers. Then, their software models will be presented, both full-scale and small-scale (equivalent of the experimental board). The results obtained in simulations and in the experimental measurements will be compared and some key conclusions will be drawn about both topologies, summarized in Table *3* – Comparison of DAB and BPSFB converters.

The deliverable has the following sections:

Section 2 defines abbreviations and acronyms used in this report.

Section 3 describes in detail the Dual Active Bridge (DAB) and the Bidirectional Phase-Shift Full-Bridge (BPSFB) converters, proposed for the MVDC Power Electronic Traction Transformer (PETT). Their mathematical models offer the basis for the PI and PID controller design. The equations and figures of this section offers an insight to converter modelling and compensator design.

Section 4 presents the full-scale simulation models of the two PETTs, one based on DAB modules and the other based on BPSFB modules. The full-scale model is scalable, a designer can choose the number of modules based on the chosen semiconductors for the converter and based on the power requirements. Here, an 8 modules system was implemented, with 1.2MW nominal power, capable of powers up to 2MW. For scalability and the calculation of component values a Mathcad automated design sheet was developed for both converter topologies, not included in this summary report.

Section 5 contains comparative figures of the experimental measurements and their simulation model. The experimental waveforms obtained are similar and very close to the values of those from simulations. As key KPIs, our converter board archives power density of 4.34MW/m3 and the difference of the current drawn by the converter between experiment and simulation is 5-10%.

Section 6 deals with the problem of losses and presents some equations useful to calculate the conduction and switching losses based on the chosen semiconductors. Some design guidelines are also included in this chapter.

Finally, section 7 draws the conclusions and section 8 includes the references.

# Abbreviations and acronyms

|  |  |
| --- | --- |
| ABB | ASEA Brown Boveri |
| AC | Alternating Current |
| DAB | Dual-Active Bridge |
| DC | Direct Current |
| EMC | Electromagnetic Compatibility |
| EMI | Electromagnetic Interference |
| ERS | Electric Railway System |
| ESR | Equivalent Series Resistance |
| FUNDRES | Future Unified DC Railway Electrification System |
| HV/MV/LV | High Voltage / Medium Voltage / Low voltage |
| IGBT | Insulated Gate Bipolar Transistor |
| ISOP | Input Series Output Parallel |
| JFET | Junction-Gate Field-Effect Transistor |
| LFT | Line/Low Frequency Transformer |
| MFT | Medium Frequency Transformer |
| MMC | Modular Multilevel Converter |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistors |
| MVDC | Medium-Voltage DC |
| PETT | Power Electronic Traction Transformer |
| PI/PID | Proportional-Integral/Proportional-Integral-Derivative controller |
| PSFB/BPSFB | Phase-Shift Full-Bridge/Bidirectional Phase-Shift Full-Bridge |
| RHP | Right Half Plane |
| RMS | Root mean square |
| Si/SiC | Silicon/Silicon Carbide |
| SMPS | Switched Mode Power Supply |
| SMW | Separated Multi-Winding |
| SST | Solid State Transformer |
| THD | Total Harmonic Distortion |
| VSD | Variable Speed Drive |
| WBG | Wide Band-Gap |
| ZCS/ZVS | Zero Current Switching / Zero Voltage Switching |

# Description of proposed converters for MVDC Power Electronic Traction Transformers

The literature review for deliverable D2.1 found that the cascaded modular ISOP configuration with separated multi-winding (SMW) isolation is currently the best PETT topological family for the MVDC railway concept. As a sub-topology for the modules, an active full-bridge converter was proposed [1]; consequently, two distinct active-bridge converters were modelled, designed, and implemented during RP2 and RP3 as contenders for the project's traction transformer. On Fig. 1, one can see the final definition of the topology from D2.1. The first converter addressed was a symmetrical dual active full-bridge converter (DAB) – presented in 3.1, while the second was a phase-shift full-bridge converter (PSFB) – presented in 3.2; both are bidirectional and widely proposed for power electronics applications.

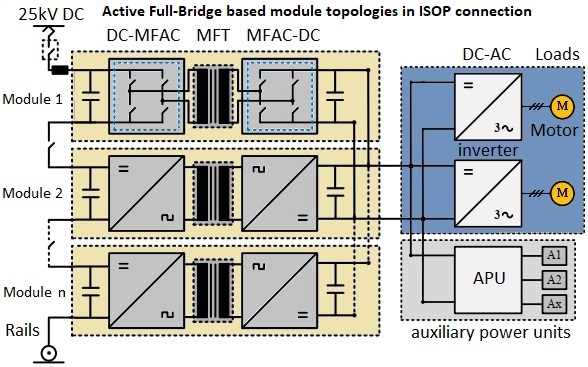


Fig. 1 – Cascaded modular ISOP connected active full-bridge converters.

## Dual Active Bridge converter

### Mathematical model

The converter equations will be derived starting from its basic waveforms [2]. As seen on Fig. 2a, for the interval 0 < t < d∙T (d being the phase shift between the two bridges), the voltage on the leakage inductor is the sum of the input voltage – noted vi , and the output voltage reflected in the primary – noted vo’ (vo’ = vo/n, where n is the transformer turn ratio). Similarly, for the interval d∙T < t < T the inductor voltage is then vi - vo’. Therefore, the inductor voltage has the following equation as a function of the value of the inductor – Llk, the half of the switching period – T, and the peak values of the inductor current – I1 and I2:

Adding (1a) and (1b) one can obtain the value of I2:

Subtracting (1b) from (1a) the other peak, I1 is obtained:

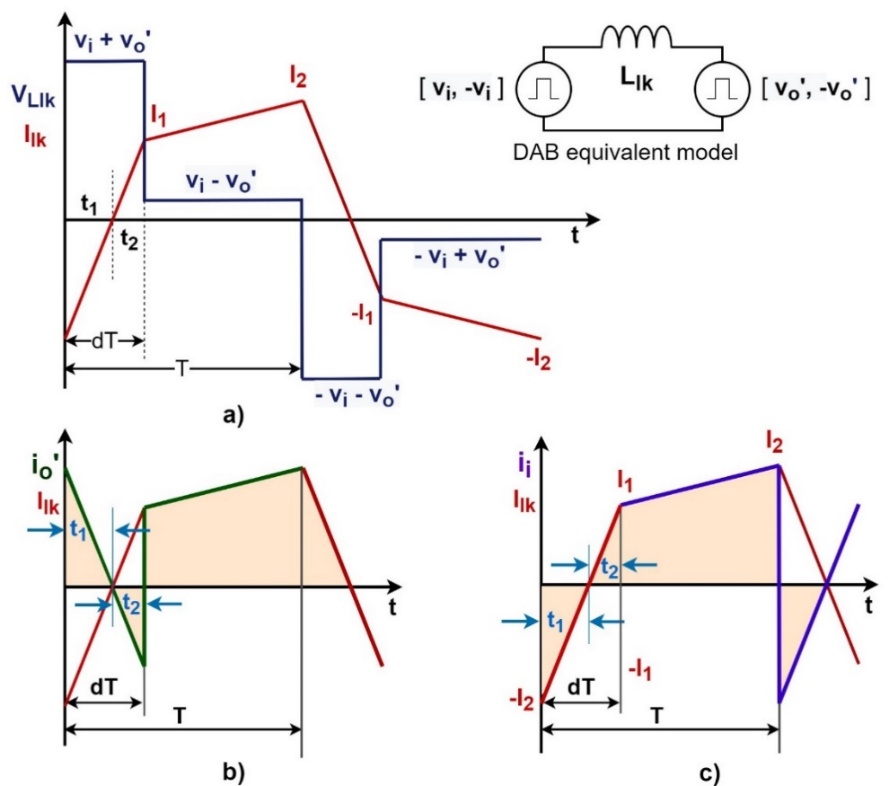


Fig. 2 – Dual Active Bridge converter - waveforms: a) presents the leakage inductor voltage and current more detailed, b) shows the output current reflected in the primary, compared to the leakage inductor current, and c) represents the input current in the same manner.

Now looking at Fig. 2b and c, d∙T is split in two subintervals, t1 and t2 with the following characteristics:

From (4), t1 and t2 can be solved, if we divide (3) with (2) and then vice-versa:

Having now the peak values and the time intervals for the leakage inductor current, the average input current can be calculated, using Fig. 2c):

Using Fig. 2c), in a similar way the average output current can be also derived:

From (2), (3) and (5)-(7) they can be rewritten as:

Having these equations, the average model is obtained [2], see Fig. 3 below.

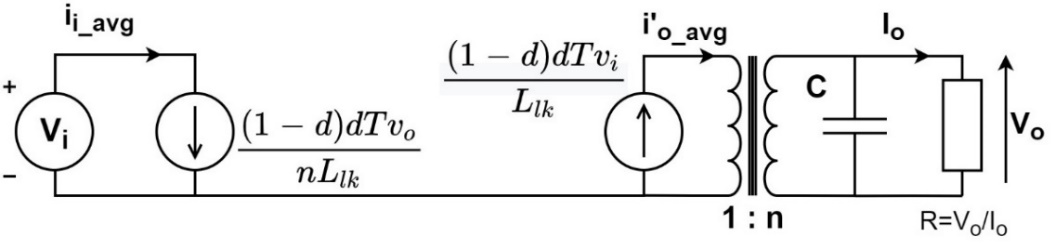


Fig. 3 – Average model of a DAB module.

Using this model, the output voltage as a function of the input voltage and the load is:

The power transferred is:

Then, from (9), the relation of the input and output voltage – the transfer ratio is obtained:

From (10) the leakage inductor can be calculated using the desired phase-shift and the maximum power. A small inductance yields maximal power transfer with a small phase-shift. To finely control power transfer, high resolution phase steps are required. Alternatively, a larger inductor can ensure maximum power transfer with improved control (higher phase-shift range).

### The small signal model

Perturbing (8), the equations of the average input and output current, and the small signal model can be derived:

Where god, gid, govi and givo are:

Now, from (12) the circuit schematic of small signal model can be drawn [2], as in Fig. 4.

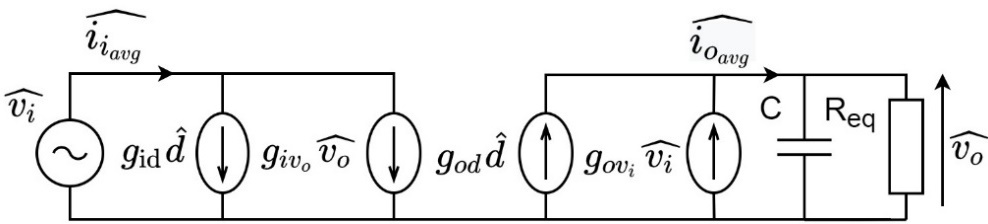


Fig. 4 – Small signal model of a DAB module.

Based on the small signal model, the variations of the output voltage as a function of the input voltage and the phase-shift is:

Substituting (13) and (15) into (16) and considering a constant input voltage, the transfer function can be obtained [3]–[6]:

The transfer function of the DAB converter and its phase plot can be seen on Fig. 5. Being a first order transfer function, a PI compensator with the following form will be a sufficient solution to control the output voltage [7], [8]:

### The PI controller design

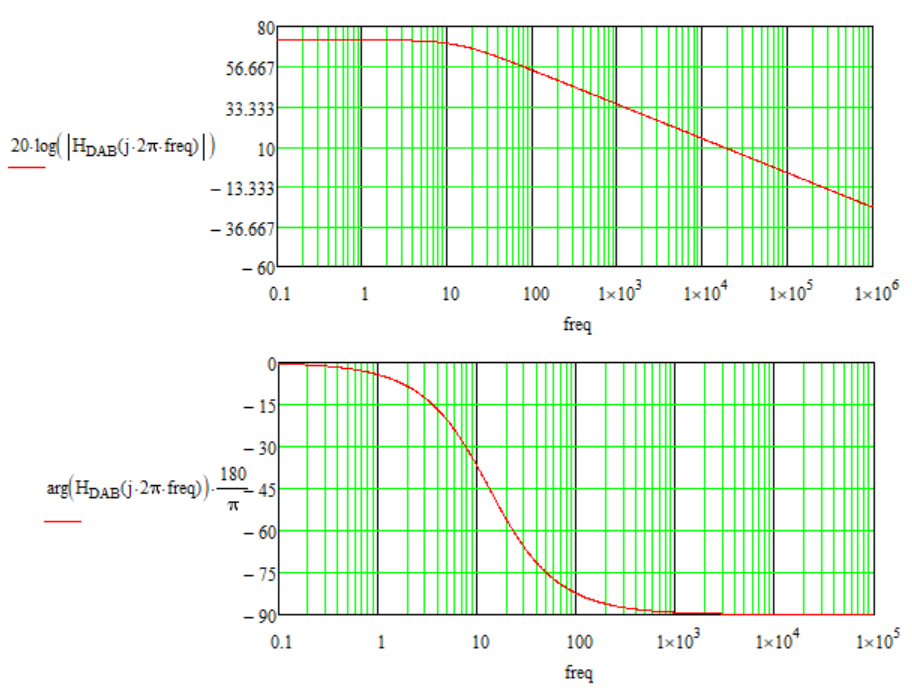


Fig. 5 – DAB module transfer function: Bode plot (magnitude and phase).

Let the cut-off frequency be fc = fsw/10 = 1kHz. At f = 1 kHz:

For stability and optimal functionality, the phase margin is chosen 70˚, or π/4, meaning:

From (21) the time constant from the PI’s transfer function can be obtained as [9]:

Then from (19):

From (23) K is obtained, which is the proportional constant:

Having both K and T, the integral constant is now straightforward, based on (18):

Finally, the transfer function of the PI compensator is:

The PI design process is automatized in Mathcad. A screenshot from the Mathcad design sheet is presented in Fig. 6. For the phase margin is set to 70 degrees and the cut-off frequency is tenth of fswitch.

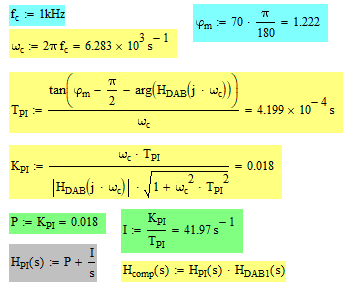


Fig. 6 – PI design equations in Mathcad.

Plotting the compensated loop’s transfer function, Hc(s)=HDAB(s)‧HPI(s) in Mathcad, the design of the PI can be verified:

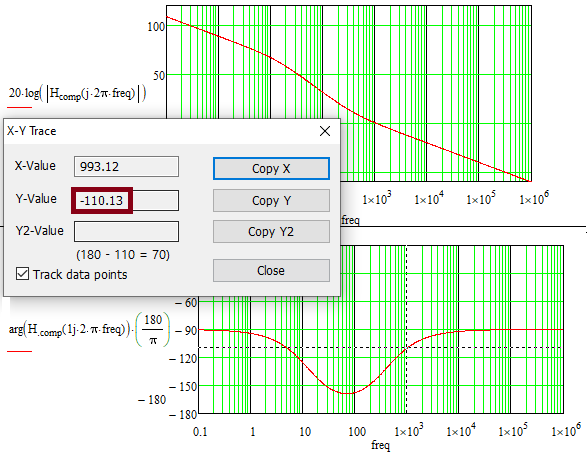


Fig. 7 – The compensated transfer function’s Bode plot and phase (at fc).

As Fig. 7 shows, the phase margin is indeed 70˚. Applying Tustin or trapezoidal discretization on (26), the compensator’s transfer function in Z domain is [7], [8]:

Where TS is a new parameter, the sampling time or sampling period, which is usually selected higher than the switching frequency. Having a 10 kHz switching frequency, TS will be 20∙10-6 s, which is corresponding to 50 kHz. Then, the transfer function in Z domain is:

Based on (26), the PI block configuration in Matlab/Simulink looks like in Fig. 8:

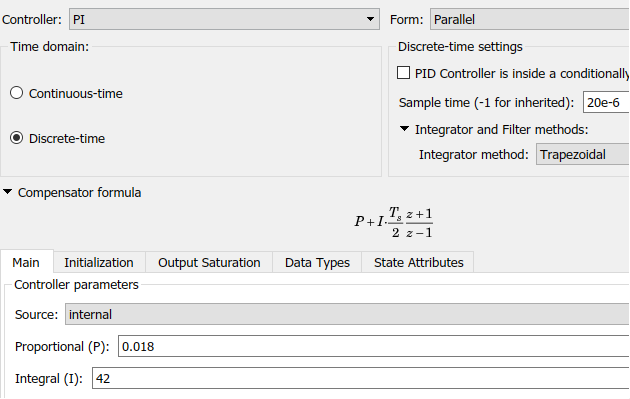


Fig. 8 – Simulink PI block configuration.

A Mathcad design sheet was developed for both converters, with all the design equations, including for the control loop as well, plots and losses estimation.

## BPSFB converters

In recent years, the trend in switched mode power supply (SMPS) has been to enhance power density while keeping costs low. High efficiency is a crucial characteristic for achieving this increased power density since heat dissipation must be kept to a minimum. For high-power, high-voltage DC-DC converters, fully resonant topologies, such as LLC, have long been regarded the optimum solution. The BPSFB topology can achieve performance levels that are comparable or equivalent. Unlike existing resonant topologies, the suggested bi-directional operation has no design constraints, has no impact on efficiency, and does not require any additional components. The converter is galvanic isolated and capable of voltage regulation over a wide range. Due to the soft switching capability on the primary side, it has high efficiency [10]–[12]. However, because a filter inductor is used on the secondary side but not on the primary, the topology is asymmetric. The high voltage spike on the secondary switching components is a problem with PSFB converters. A diode clamp circuit is a frequent solution to this problem [13], [14].

Some advantages of the BPSFB converter:

* On the positive power flow direction, it has zero voltage switching (ZVS) characteristics; on the negative power flow direction, it has zero current switching (ZCS) characteristics
* High efficiency performance can be obtained regardless of the direction of power flow and it performs well in terms of stability and dynamic response

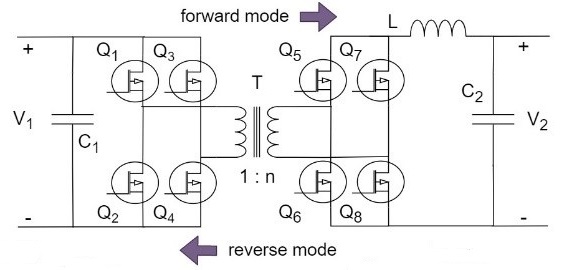


Fig. 9 – The bidirectional phase-shift full-bridge converter circuit.

### Mathematical model

The BPSFB topology is asymmetric, as shown in Fig. 9. When the voltage is converted from V1 to V2, the converter is a voltage mode full-bridge converter. When the voltage is transferred from V2 to V1, where V1 denotes high voltage and V2 denotes low voltage, it is a current mode full-bridge converter. The circuit contains nonlinear elements such as power switches and diodes, making it a nonlinear time-varying system. To obtain the converter model, it is necessary to use mathematical methods to simplify the complex physical model. The small-signal analysis method is appropriate for linearising nonlinear systems and obtaining transfer functions. The closed-loop controller will then be designed using classical control theory.

This topology is basically a galvanically isolated buck-boost converter, from the operation point of view [15]. Therefore, the forward mode (voltage mode) will be equivalent to a Buck converter, with the ratio of the transformer (1:n) added into the circuit. Fig. 10 presents the equivalent circuit. On the other hand, in backward mode (current mode) the energy transfer is the same as in a Boost converter. See the equivalent circuit in Fig. 11.

#### Forward mode (Buck equivalent)

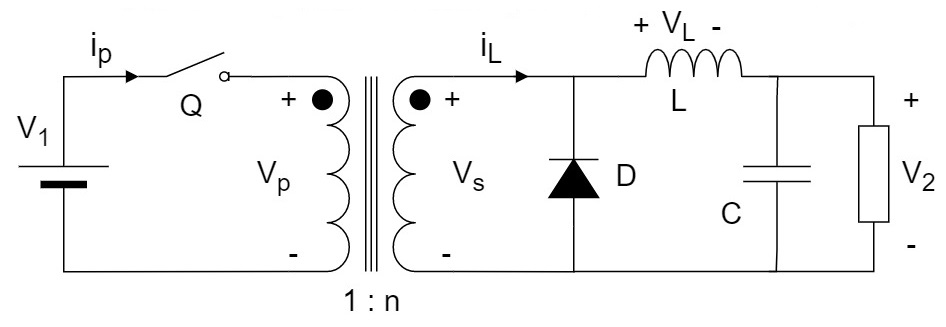


Fig. 10 – BPSFB forward mode equivalent circuit.

Since the Buck converter’s mathematical model is well known, it will not be deduced here. See the open loop input to output transfer function for this voltage controlled converter in the next equation.

Then, the control to output transfer function is:

#### Backward mode (Boost equivalent)

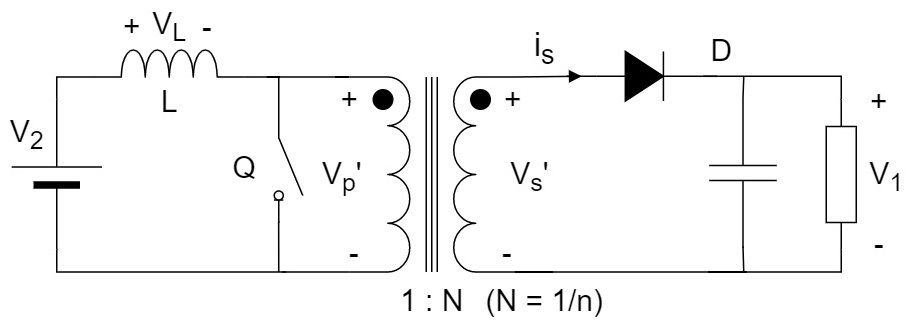


Fig. 11 – BPSFB backward mode equivalent circuit.

In the same way, since the boost converter is well known as well, its transfer function will not be deduced here. See the control to output transfer function in the following equation.

The transfer function, (32), consists of a double-pole, right half plane (RHP)-zero and equivalent series resistance (ESR)-zero. See their equation and damping factor – Q in (33).

Variable N here is 1/n, the inverse of the transformer turn ratio and D is the duty cycle. See the difference by comparing Fig. 10 and Fig. 11. Since it is a second order transfer function, a PID controller is necessary to achieve stability in the case of the BPSFB converter.

### PID compensator design

Before designing the control loop, the PID parameters will be deduced, using frequency-domain methods [9]. The transfer function of a PID controller can be either in additive or multiplicative form. Additive form of a filtered PID’s transfer function is as follows:

Multiplicative form of a PID transfer function is stated as:

The two forms are equivalent. For tuning the PID controller, its coefficients can be determined based on the following initial conditions and parameters:

1. The phase margin
2. , where
3. The frequency of the zero introduced by the integrative part has to be sufficiently small not to affect the phase (arg(T(jωc))) of the open loop transfer function at cut-off frequency fc. It is recommended to be set: .
4. The frequency of the pole introduced by the derivative part is recommended to be . This however, can be changed as necessary.

The first condition: the phase margin can be defined as:

Second condition:

From (40) and after rearrangement, the integrative coefficient is obtained:

Applying these constrains all the coefficients of the PID controller can be obtained. In order to do so, the multiplicative and additive forms have to be equated. The multiplicative form from (35), with solved brackets in the numerator:

The additive form solved:

Having the parameters are the following:

From (44), kI being kPID and knowing Tf, the other two PID coefficients can be obtained as well:

The z domain form after Tustin discretisation of the filtered PID, :

This transfer function is more difficult to be arranged into the form of:

After several steps, however, the discrete transfer function of a filtered PID will have the following form:

The differential equation of this is:

,where ; ; ;

; and . This now can be implemented in C or other programming language as well. See the PID block configuration window from Simulink on Fig. 12.

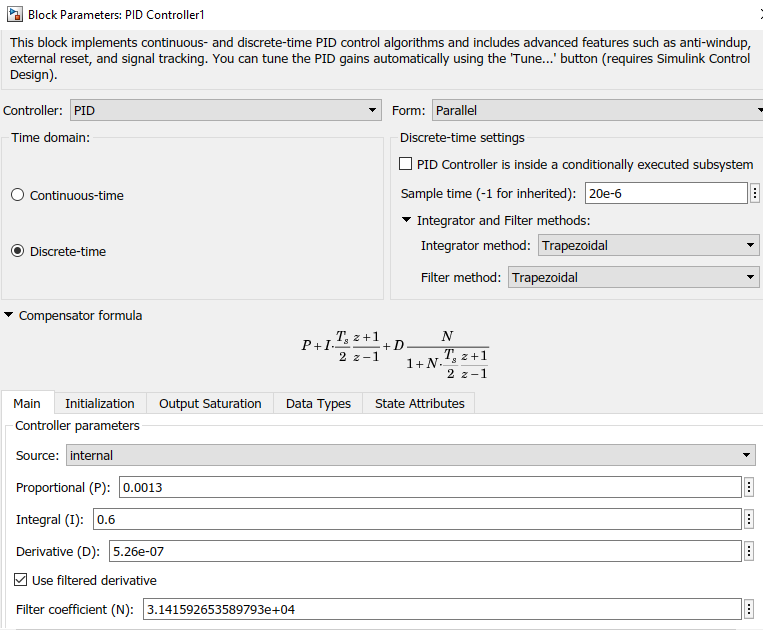


Fig. 12 – Discrete domain PID block in Matlab/Simulink.

For simplicity, in the Mathcad design sheet and for the calculation of the PID parameters, the inductor parasitic resistance will be ignored and only the ESR capacitor parasitic resistance will be included in the transfer function of the two operation modes. Therefore, the following form of equations (30) and (32) will be used in the implementation of the control loop:

The design process is similar as described in 3.1.3. The gain and the argument of the transfer function for the Buck operation mode is shown in Fig. 13 and for the Boost mode in Fig. 14. The tuning of the PID compensator starts from the four initial conditions presented previously and then equations (39), (41), (45) and (46) are applied. A screenshot of the design equations in Mathcad is presented in Fig. 15. A similar tool for PID parameter design was developed in Matlab as well – a script that plots and calculates all the compensator parameters, based on the transfer functions of the converter from (51) and (52). In the project both tools were used to implement the full scale system’s and the small scale experimental board’s simulation models.

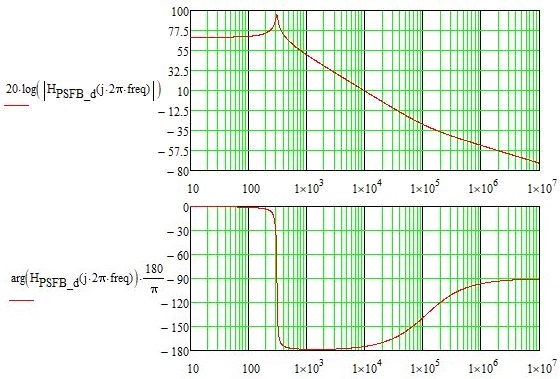


Fig. 13 – Bode plot of BPSFB converter – Buck mode.

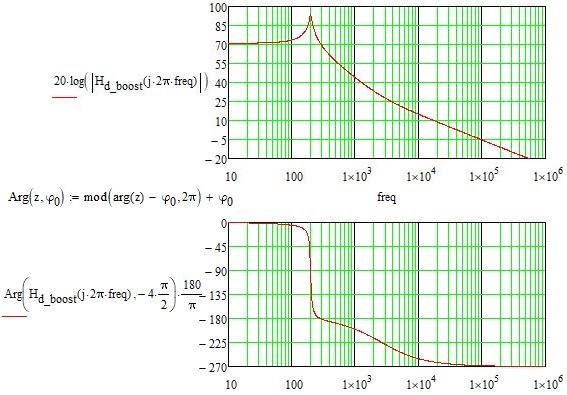


Fig. 14 – Bode plot of BPSFB converter – Boost mode.

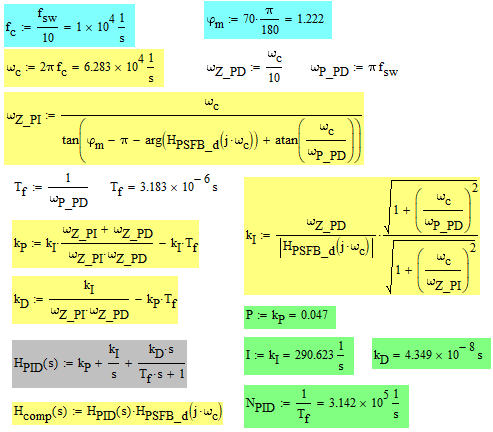


Fig. 15 – Design equations resulting the tuning parameters.

# Full-scale simulation model of the PETTs

Based on the mathematical model of the converters, using the Mathcad automated design sheets, a single module was implemented of both converter sub-topologies, first in PSIM software, then in Matlab/Simulink as well. After successful simulation of the converter modules, in the second phase of the software model’s implementation a full-scale eight module version of the traction transformer was developed. Finally, in the experimental phase of the project, another exact model of the experimental converter board was implemented in Simulink to compare results from the oscilloscope with the one obtained from simulations.

## DAB converter based PETT

Table 1 represents the MVDC railway line parameters defined in D1.1 and D1.2, also men-tioned in D2.1 [1], [16], [17]. The full-scale PETT based on DAB converter modules presented in Fig. 16 was tested against the whole range of possible voltages of the catenary line.

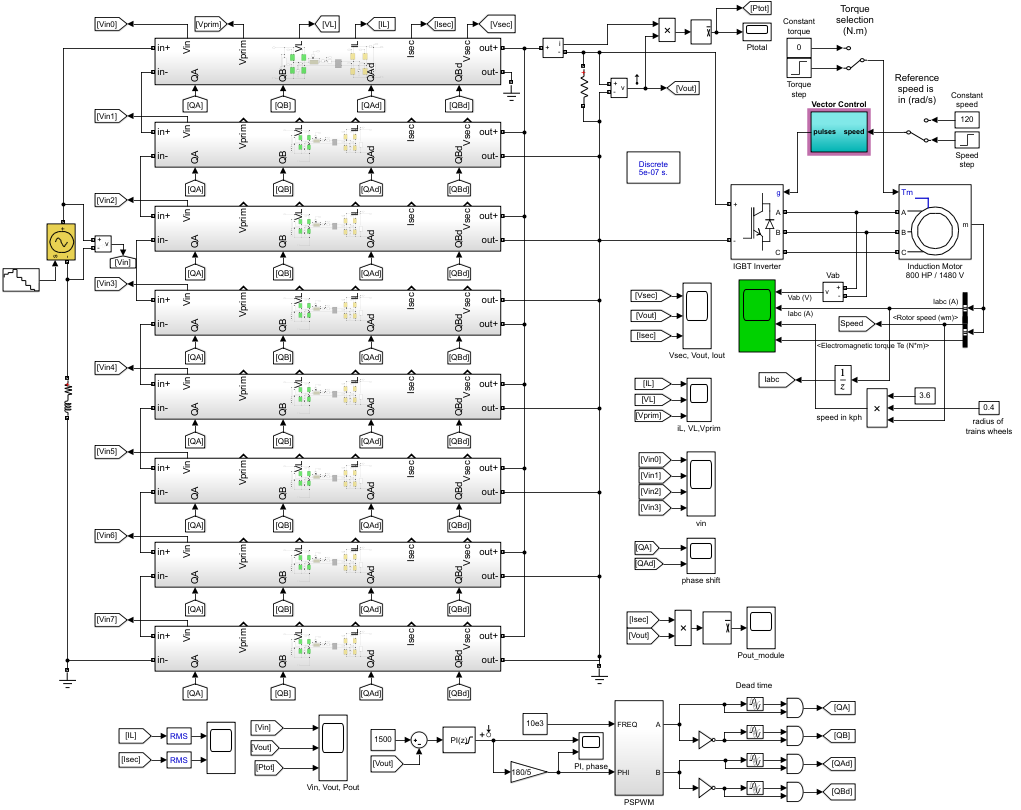


Fig. 16 – The 8 module DAB based PETT system. Input variations simulation model.

Table 1 – Input voltage specifications for PETT (catenary line voltages).

|  |  |  |
| --- | --- | --- |
| Parameter | Symbol | Value (kV) |
| Lowest non-permanent voltage |  | 17.5 |
| Lowest permanent voltage |  | 19 |
| Nominal voltage |  | 25 |
| Highest permanent voltage |  | 27.5 |
| Highest non-permanent voltage |  | 29 |

In the simulation model different input voltage variations were simulated from 17.5kV up to 29kV with different step sizes. The designed votlage control loop can keep the output votlage and output power constant on the whole range as Fig. 17 illustrates.

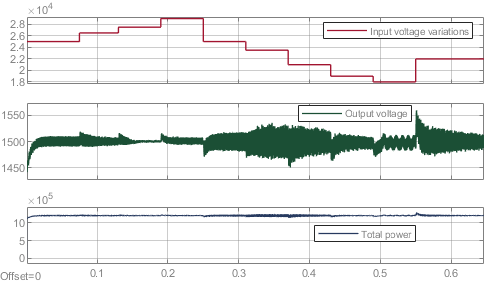


Fig. 17 – Ten different voltage levels from the lowest to the highest non-permanent catenary voltage.

In the same model some load steps were simulated as well. See the total power for five load steps in Fig. 18 and the secondary waveforms as a function of those load steps in Fig. 19. The total maximum nominal power is 1.2MW in this model.

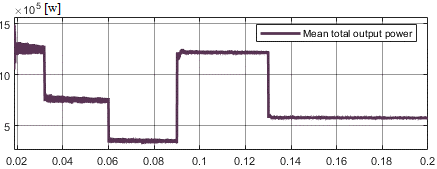


Fig. 18 – Total output power of the PETT: Maximum power and different load steps.

As it can be observed on Fig. 17 and Fig. 19, the response of the system is good and the controlled quantity, i.e., the output voltage, is kept at 1500 V with less than 10% transient voltage. The voltage ripple is below 5% for both input voltage and load steps.

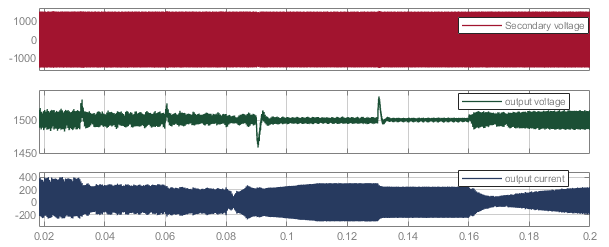


Fig. 19 – Secondary voltage and output waveforms as a function of load steps.

## BPSFB converter based PETT

The same simulations for the PSFB based version of the PETT – Fig. 20, are shown on the following figures. The output voltage and power response to the input voltage steps in the whole range from Table 1 is presented on Fig. 21. In these simulations, the output voltage ripple is smaller in the case of PSFB converter modules based traction transformer system, compared to the DAB modules based system. However, a higher overshoot can be observed at large step variations of the input voltage in the output voltage. The phase-shift converter is a second order system and it is controlled with a PID controller, which has to be designed more carefully, to cover the whole range of possible input parameter variations.

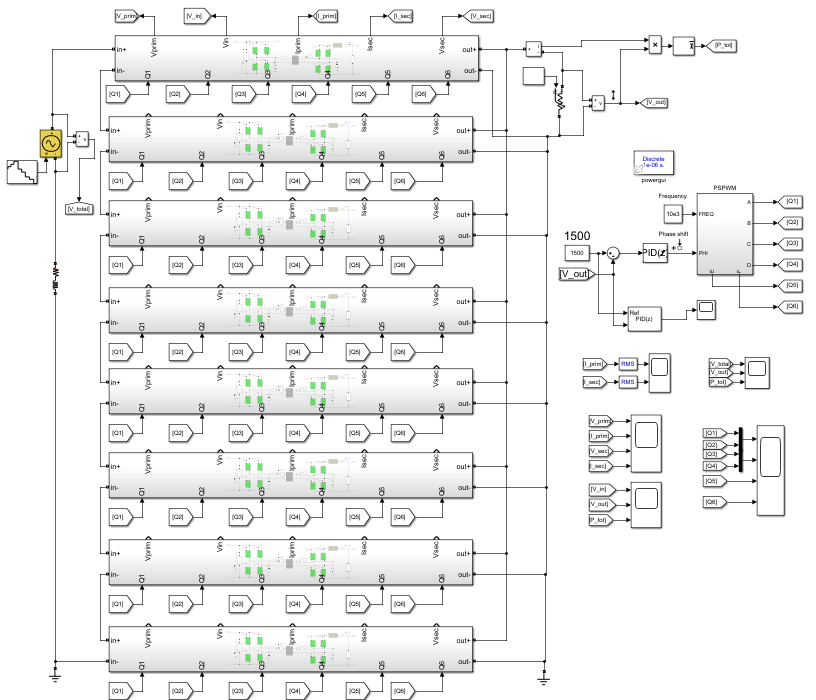


Fig. 20 – The 8 module PSFB based PETT system. Input and load variations simulation model.

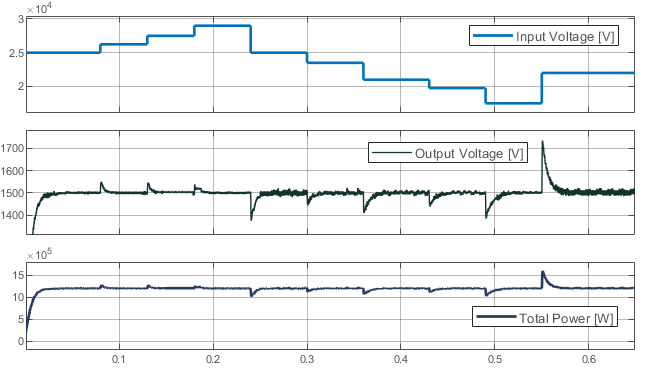
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Fig. 21 – Input voltage steps from the lowest to the highest non-permanent catenary voltage in the case of BPSFB converter based PETT system.

According to the simulations, this converter topology however, has a smoother response for the load variations, with minimal output ripple. Fig. 22 illustrates the input and output voltage against different load steps.

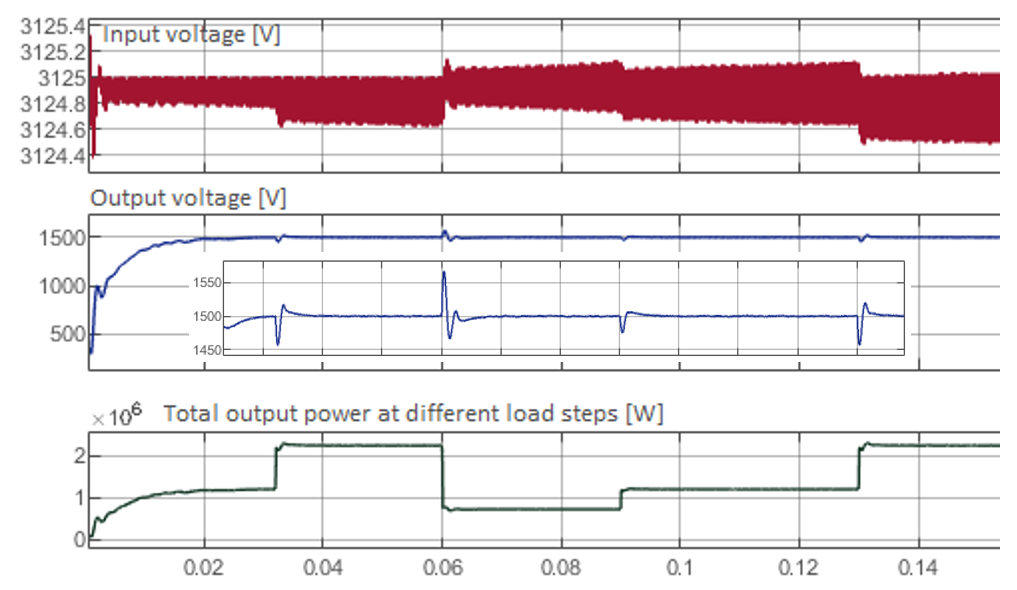


Fig. 22 – The regulated quantity (output voltage) in the case of BPSFB converter as a function of load steps (in the middle). Down with green the total output power can be observed and in the upper part the module input voltage. The output voltage ripple in the case of the PSFB converter is smaller.

The chosen traction motor to test if it can be operated successfully in different modes, is an 800HP, 1480V nominal voltage three phased asynchronous induction motor. It can be seen on Fig. 16. The system motor is vector controlled in the dq rotary reference system, having an input speed regulator and an output current regulator. A step in torque and speed was simulated and it can be observed on the scope on Fig. 23. On the left side, the rotor speed is first stabilised at 160 rad/s, then a torque step occurs at 1.8 seconds. The change of Iabc currents follows the torque. On the right side, an acceleration, then maintaining speed can be observed.

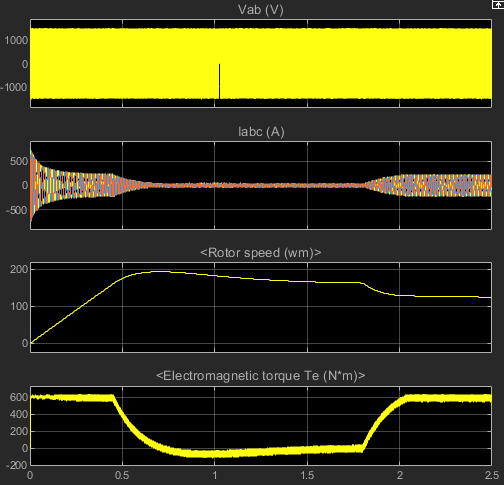
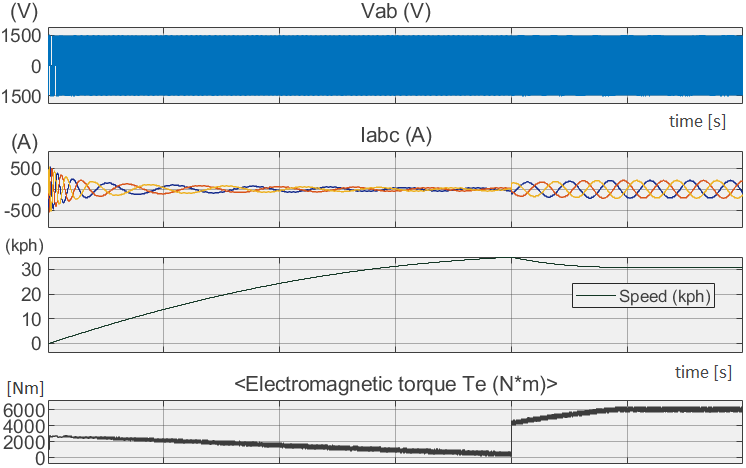
**

Fig. 23 – Traction motor waveforms.

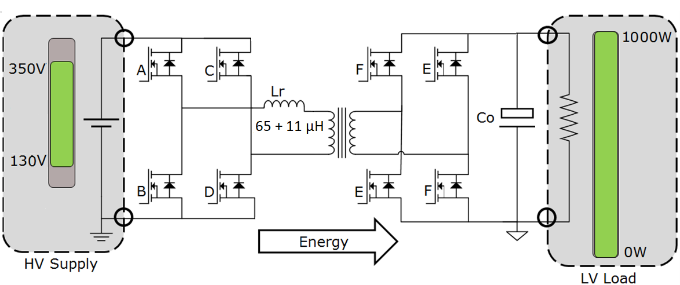
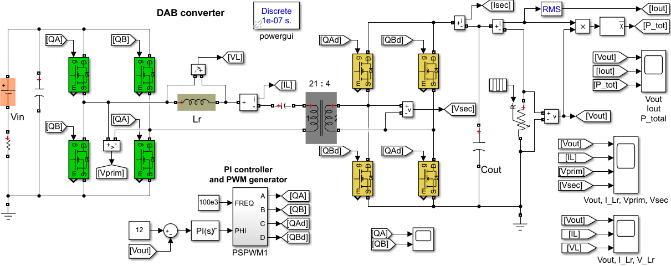
The focus of WP2 is on the PETT system and as a basic simulation of an attached motor demonstrates, it operates stable in different operation modes of the traction motor.

# Small-scale experimental prototype of the PETTs

Both modules were implemented and put to the test experimentally as a result of two successful full-scale simulation models. The small-scale prototype is a modified bidirectional PSFB converter board that has been modified into a DAB converter. Both topologies were evaluated, and measurements were compared to the Matlab/Simulink simulation model of both converters.

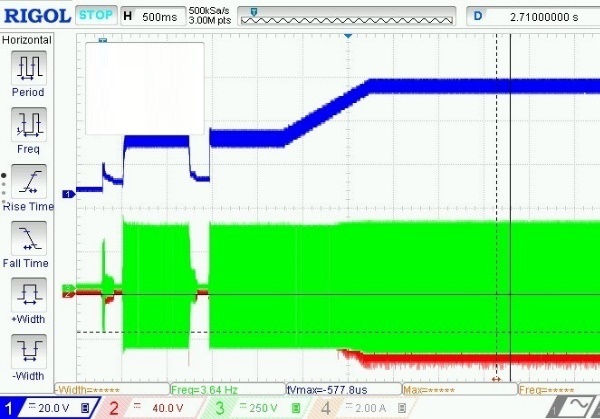
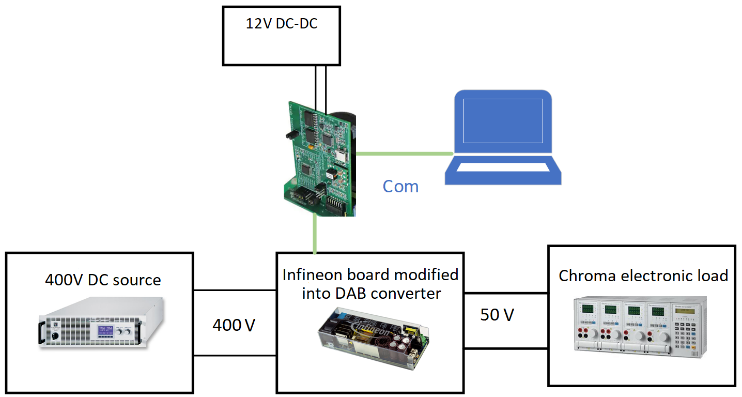
## Dual Active Bridge module

The DAB module is presented on Fig. 24 – the schematic of the converter module on the left and its Matlab/Simulink model (with the same parameters) on the right. The converter was tested between 130-350V input voltage and 0-1000W output power. For the results presented here, see the experimental setup on Fig. 25. The converter was controlled digitally, using a Texas Instruments control board, and as load, a Chroma electronic load was attached to the system. Waveforms for two different loads and response to load steps will be presented in the following to compare experiments with the simulation.

1. *(b)*

Fig. 24 – Small-scale DAB module (a) and its simulation model (b).



1. *(b)*

Fig. 25 – a) Experimental setup of the DAB PETT module. b) Soft start of the converter with 300 ns dead time: channel 1 – Vo (output voltage), ch. 2 – Vsecondary (secondary voltage) and on ch. 3 – Vprimary.

The soft start of the converter can be seen on Fig. 25b. Then, Fig. 26 shows some key waveforms at 6A load current. Fig. 26 presents the output voltage variation, inductor current, primary and secondary voltages waveforms at 300W output power. To deliver power at different rates, the phase-shift between the two bridges is modified, which affects the resonant inductor’s current and voltage waveforms. Fig. 27 and Fig. 28 presents the inductor current and voltage along with the output voltage for two different loads, 6A and 2A – 300W and 100W respectively.

Fig. 26 – a
 Waveforms at 6A load current. (a) on the oscilloscope: channel 1 – ΔVO (output volt-age ripple), ch.2 – VSec, ch.3 – VPrim, ch.4. – resonant inductor current ILr;  Fig. 26 – b

Waveforms at 6A load current. (a) on the oscilloscope: channel 1 – ΔVO (output volt-age ripple), ch.2 – VSec, ch.3 – VPrim, ch.4. – resonant inductor current ILr; (b) the same in the simulation model.

1. *(b)*

Fig. 26 – Waveforms at 6A load current. (a) on the oscilloscope: channel 1 – ΔVO (output voltage ripple), ch.2 – VSec, ch.3 – VPrim, ch.4. – resonant inductor current ILr; (b) the same in the simulation model.

Fig. 27 – a
Waveforms at 6A load current. (a) on the oscilloscope: ch.1 – ΔVO, ch.3 – primary inductor voltage VLp, ch.4. – resonant inductor current ILr; (b) same waveforms in the simula-tion model.Fig. 27 – b
Waveforms at 6A load current. (a) on the oscilloscope: ch.1 – ΔVO, ch.3 – primary inductor voltage VLp, ch.4. – resonant inductor current ILr; (b) same waveforms in the simula-tion model.

1. *(b)*

Fig. 27 – Waveforms at 6A load current. (a) on the oscilloscope: ch.1 – ΔVO, ch.3 – primary inductor voltage VLp, ch.4. – resonant inductor current ILr; (b) same waveforms in the simulation model.

Fig. 28 –a
 Waveforms at 2A load current. (a) on the oscilloscope: ch.1 – ΔVO,  ch.3 – primary inductor voltage VLp, ch.4. – resonant inductor current ILr; (b) same waveforms in the simula-tion model.Fig. 28 – b
Waveforms at 2A load current. (a) on the oscilloscope: ch.1 – ΔVO,  ch.3 – primary inductor voltage VLp, ch.4. – resonant inductor current ILr; (b) same waveforms in the simula-tion model.

1. *(b)*

Fig. 28 – Waveforms at 2A load current. (a) on the oscilloscope: ch.1 – ΔVO, ch.3 – primary inductor voltage VLp, ch.4. – resonant inductor current ILr; (b) same waveforms in the simulation model.

Finally, the system’s response to load steps (2A – 100W) are tested – from 2A to 4A. Fig. 29(a) is a screenshot of the oscilloscope, while (b) is from the simulation model, where the power variation was included as well. The converter is stable with a fast response.

Fig. 29 – a
Response to load steps: (a) ch.1 – ΔVO, ch.4 – IO (2A/division); (b) in the simulation model.

(a)

Fig. 29 – b
Response to load steps: (a) ch.1 – ΔVO, ch.4 – IO (2A/division); (b) in the simulation model.

(b)

Fig. 29 – Response to load steps: (a) ch.1 – ΔVO, ch.4 – IO (2A/division); (b) in the simulation model.

A speed profile was done in the experiment, while measuring the motor and control currents. See the experimental setup and the obtained results on Fig. 30 and Fig. 31 respectively.

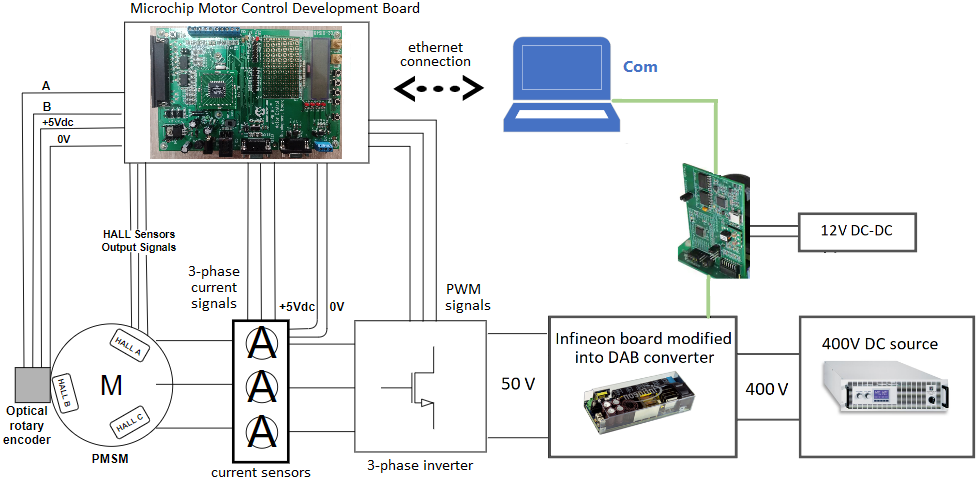


Fig. 30 – Laboratory experiment – Motor drive setup block diagram.



Fig. 31 – Laboratory experiment measurements – Motor drive speed profile and current waveforms.

The DAB module is a simple, yet powerful converter and it presented a stable operation for different scenarios and it would be suitable for a modular PETT system. More conclusions will be drawn in the conclusion section.

## Bidirectional Phase-Shift Full-Bridge module

For the BPSFB module the same approach was used. Fig. 32(a) shows the converter scheme and (b) its simulation model with the same parameters as in the experiment. See the detailed specifications of the board in Table 2 and the experimental setup on Fig. 33. Due to the output inductor, this converter is a second order system and it is controlled differently compared to the DAB. This converter is controlled digitally with an Infineon board using a computer software to set the PID parameters. To test the system above 1000W and to simulate 500W load steps, two electronic loads were attached to the converter in this experimental setup, as seen on Fig. 33(a). The soft start of the module can be seen in Fig. 33(b).

Fig. 32 – a
Small-scale BPSFB module (a) and its Matlab/Simulink model (b).

(a)

Fig. 32 – b
Small-scale BPSFB module (a) and its Matlab/Simulink model (b).

(b)

Fig. 32 – Small-scale BPSFB module (a) and its Matlab/Simulink model (b).

Table 2 – Converter board specifications [13].

| Small-scale module board and its simulation model specifications | | |
| --- | --- | --- |
| Input voltage range: Vin\_min – Vin\_max | 350-400 | V |
| Output voltage: Vout (and Vnominal) | 47-60 (50 nominal) | V |
| Output power: Pout (and Pout\_max) | 1000 (max 3300) | W |
| Maximum output current: Iout\_max | 85 | A |
| Switching frequency: fsw | 100 | kHz |
| Transformer turn ratio: n = Nprim/Nsec | 21/4 = 5.25 | - |
| Maximum duty cycle: Dmax | 82 | % |
| Magnetizing inductance: Lmag | 750 | µH |
| Resonant inductor: Lr | 11 (11+65 for DAB) | µH |
| Output inductor: Lo | 9.8 | µH |
| Dead time | 300 | ns |

Fig. 33 – a
a) Experimental setup of the BPSFB PETT module. 
b) Soft start of the converter: channel 1 – Vo (output voltage), ch. 2 – Vsec (secondary voltage).


*(a)*

Fig. 33 – b
a) Experimental setup of the BPSFB PETT module. 
b) Soft start of the converter: channel 1 – Vo (output voltage), ch. 2 – Vsec (secondary voltage).


*(b)*

Fig. 33 – a) Experimental setup of the BPSFB PETT module.   
b) Soft start of the converter: channel 1 – Vo (output voltage), ch. 2 – Vsec (secondary voltage).

On the next figure, two load scenarios will be presented. On the left column, Fig. 34 shows the output parameters for (a) 5A load current and 250W output power, (b) the waveforms on the oscilloscope – output and secondary voltage, inductor current; and (c) the same in the simulation model. The right column is identical, but for 20A load current and 1kW output power.

Fig. 34 – a1
Waveforms at 5A (a1) load current and 20A (a2) respectively: (b) on oscilloscope: ch.1 – ΔVO, ch.2 – Vprim, ch.4. – resonant inductor current ILr; (c) same waveforms in the simulation model. Fig. 34 – a2
Waveforms at 5A (a1) load current and 20A (a2) respectively: (b) on oscilloscope: ch.1 – ΔVO, ch.2 – Vprim, ch.4. – resonant inductor current ILr; (c) same waveforms in the simulation model.

*(a)*

Fig. 34 – b1
Waveforms at 5A (a1) load current and 20A (a2) respectively: (b) on oscilloscope: ch.1 – ΔVO, ch.2 – Vprim, ch.4. – resonant inductor current ILr; (c) same waveforms in the simulation model. Fig. 34 – b2
Waveforms at 5A (a1) load current and 20A (a2) respectively: (b) on oscilloscope: ch.1 – ΔVO, ch.2 – Vprim, ch.4. – resonant inductor current ILr; (c) same waveforms in the simulation model.

*(b)*

Fig. 34 – c1
Waveforms at 5A (a1) load current and 20A (a2) respectively: (b) on oscilloscope: ch.1 – ΔVO, ch.2 – Vprim, ch.4. – resonant inductor current ILr; (c) same waveforms in the simulation model. Fig. 34 – c2
Waveforms at 5A (a1) load current and 20A (a2) respectively: (b) on oscilloscope: ch.1 – ΔVO, ch.2 – Vprim, ch.4. – resonant inductor current ILr; (c) same waveforms in the simulation model.

*(c)*

Fig. 34 – Waveforms at (a) 5A load current and 20A respectively: (b) on oscilloscope: ch.1 – ΔVO, ch.2 – Vprim, ch.4. – resonant inductor current ILr; (c) same waveforms in the simulation model.

The response for load steps was tested with 100ms and 10A (500W) steps, see Fig. 35.

Fig. 35 – a
Response to 100 ms load steps: (a) ch.1 – ΔVO, ch.4 – IO steps;
 (b) simulation model waveforms.
Fig. 35 – b
Response to 100 ms load steps: (a) ch.1 – ΔVO, ch.4 – IO steps;
 (b) simulation model waveforms.


1. *(b)*

Fig. 35 – Response to 100 ms load steps: (a) ch.1 – ΔVO, ch.4 – IO steps;  
 (b) simulation model waveforms.

### Reverse mode

In order to test the system in boost mode, the experimental setup on Fig. 36(a) was set:

Fig. 36 – a
a) Experimental setup of the BPSFB PETT module for backward (boost) mode. 
b) Start-up of the converter: channel 1 – Vo, ch. 2 – Vsec and ch. 4 – ILr (resonant inductor cur-rent).
 **Fig. 36 – b
a) Experimental setup of the BPSFB PETT module for backward (boost) mode. 
b) Start-up of the converter: channel 1 – Vo, ch. 2 – Vsec and ch. 4 – ILr (resonant inductor cur-rent).
**

1. *(b)*

Fig. 36 – a) Experimental setup of the BPSFB PETT module for backward (boost) mode.   
b) Start-up of the converter: channel 1 – Vo, ch. 2 – Vsec and ch. 4 – ILr (resonant inductor current).

Then, in the following, Fig. 37 shows two cases, 500W and 1kW power transfer in backward mode. Part (a) of the figure shows the parameters from the electronic load, voltage, current and power, then part (b) and (c) the key waveforms. Fig. 38 presents a 1A load step response.

Fig. 37 – a1
Waveforms at 500W (a1) and 1kW (a2) respectively: (b) on oscilloscope: ch.1 – VO, ch.2 – rectified voltage, ch.4. – resonant inductor current ILr; (c) ch. 1 – VO, ch. 2 – Vprim  and ch. 4 – ILr . Fig. 37 – a2
Waveforms at 500W (a1) and 1kW (a2) respectively: (b) on oscilloscope: ch.1 – VO, ch.2 – rectified voltage, ch.4. – resonant inductor current ILr; (c) ch. 1 – VO, ch. 2 – Vprim  and ch. 4 – ILr .

*(a)*

Fig. 37 – b1
Waveforms at 500W (a1) and 1kW (a2) respectively: (b) on oscilloscope: ch.1 – VO, ch.2 – rectified voltage, ch.4. – resonant inductor current ILr; (c) ch. 1 – VO, ch. 2 – Vprim  and ch. 4 – ILr . Fig. 37 – b2
Waveforms at 500W (a1) and 1kW (a2) respectively: (b) on oscilloscope: ch.1 – VO, ch.2 – rectified voltage, ch.4. – resonant inductor current ILr; (c) ch. 1 – VO, ch. 2 – Vprim  and ch. 4 – ILr .

*(b)*

**Fig. 37 – c1
Waveforms at 500W (a1) and 1kW (a2) respectively: (b) on oscilloscope: ch.1 – VO, ch.2 – rectified voltage, ch.4. – resonant inductor current ILr; (c) ch. 1 – VO, ch. 2 – Vprim  and ch. 4 – ILr .** **Fig. 37 – c2
Waveforms at 500W (a1) and 1kW (a2) respectively: (b) on oscilloscope: ch.1 – VO, ch.2 – rectified voltage, ch.4. – resonant inductor current ILr; (c) ch. 1 – VO, ch. 2 – Vprim  and ch. 4 – ILr .**

*(c)*

Fig. 37 – Waveforms at (a) 500W and 1kW respectively: (b) on oscilloscope: ch.1 – VO, ch.2 – rectified voltage, ch.4. – resonant inductor current ILr; (c) ch. 1 – VO,ch. 2 – Vprim  and ch. 4 – ILr .

Diagram

Fig. 38 – 1A load steps in reverse mode

Fig. 38 – 1A load steps in reverse mode.

## Discussion of the experimental results

The BPSFB converter presents a stable operation as well and fast response to load steps (see Fig. 35b). It can be concluded, that both converters are good solutions for high-efficiency cascaded modular PETT for the new railway systems. The concept of this smart railway network is worthy to be further researched. The new concept is still under development and it can lay the foundation of future railway networks, which will include green energy farms and small DC smart-grids as well.

After analysing the measurements, it was concluded that for the DAB topology an output voltage ripple between 2.5% and 3.3% was obtained in the simulation model and 5% ripple on the oscilloscope in the actual experiment. The maximum difference between the currents measured in simulations compared to the experimental tests for different load scenarios were 5-10%.

In the case of the Bidirectional Phase-Shift Full-Bridge converter the maximum difference between currents is around 10% at maximum load and up to 5% for light loads. The ripple on the output voltage in the experiment is only 300mV of 50V (0.6%) for constant power. In different load scenarios with varying power the ripple reaches a maximum of 10% (5V peak to peak). In the simulation the output voltage ripple was negligible.

The experimental small-scale module prototype of PETT has 4.34 kW/L or 4.34 MW/m3 power density [13]. As additional reference, another bidirectional power converter module from the same manufacturer reached 3 MW/m3 (5.5 kW/kg). However, to better estimate the power density of a full-scale system, the state of the art literature was studied to find specific volume occupancy results on similar full scale systems and prototypes implemented by other research groups and the industry. In the transportation industry some papers present results up to 20 MW/m3 and even up to 40 kW/kg, using SiC devices and high performance inductors. Therefore, depending on the specifications, design and implementation technology, a specific volume occupancy between 10 and 20 MW/m3 is estimated for a full scale MVDC PETT. A more detailed review on power density and efficiency is included in the next chapter.

# Power losses and performance evaluation

For a power converter, power losses are mainly due to conduction and switching losses, which are dependent on the ratings and switching characteristics of the semiconductor devices and the modulation.

## Losses of DAB converter

The leakage inductance has an effect on the current. Using equations (2) and (3) – the current peaks I1 and I2 from Fig. 2, the primary RMS current and secondary RMS current is obtained:

### Conduction losses

Equation (53) show the RMS currents across the primary and secondary side. As an addition to what has been discussed earlier related to (10), it is noted that a high value of leakage inductance can contribute to soft switching up to a very low power level (on an extended power range) and hence leads to better switching performance. Alternatively, increasing the leakage inductance leads to increased RMS currents in the primary and secondary of transformer (since the currents are directly proportional with the phase-shift), switch currents, and ripple currents in the capacitor. This means, that for a given value of phase shift and inductance, the capacitance required to contain voltage ripple to a specified limit, increases as the leakage inductor's value increases. As the RMS value of capacitor current increases, the capacitor's equivalent series resistance (ESR) dissipates more energy, meaning more loss. To sum up, there exists a trade-off between an optimal value of leakage inductance to affect ZVS and minimizing conduction losses [26].

To calculate conduction losses some equations are needed. First, the primary peak current is:

Since the duty cycle operates at 0.5, let II = IP. In this case, the current flowing through the primary and secondary switches:

Primary and secondary diode average currents:

The conduction losses across the four primary side and secondary side MOSFETs can now be calculated using the MOSFET drain-source (DS) resistance – RDSon, and the forward voltage drop across their body diode – VfwD, from the datasheet.

### Switching losses

In order to determine switching losses, the switching loss curves provided by the semiconductor manufacturers are used. These are usually some figures in the datasheet of the MOSFET, showing the turn-off and turn-on energy curve, where the two axis are the Drain to Source current and switching loss in mJ. The turn-on or turn-off energy (Eon or Eoff) can be read from those graphs. Since the MOSFETs turn on at zero voltage, only the turn off loss coefficients are used for calculating the switching losses [26]. The secondary and primary turn-off switching losses therefore will be:

In (58), IP and IS are the primary and secondary current peaks or maximum values of the current, from (54). IS is n times IP. The nominal voltage and current Vnom and Inom are obtained from the data sheet. In addition to the losses from (57) and (58), two of the primary's switches turn on at voltages other than zero, resulting in switching losses during turn on. This is because the stored energy of the inductor (0.5 Li2) at this time is insufficient to discharge the capacitive energy (0.5 CV2) at the MOSFETs' output. These losses are calculated in the same way as calculated previously, but the turn on loss coefficients are taken. Thus, the total turn-on primary non-ZVS losses:

### ZVS of the DAB converter

From (2), (3), (10) and (11) Fig. 39 can be plotted, which illustrates the relation between the ZVS region, the value of the leakage inductor, previously discussed, and the voltage transfer ratio. It demonstrates that the soft switching range of the converter is maximised when the turn ratio is designed so that the primary voltage is equal to the reflected secondary voltage. In this situation, the voltage transfer ratio is equal to one, and all switches on both the main and secondary sides experience soft switching. In order for switches to turn on at zero voltage, however, the total capacitance of the switching node must be discharged by currents I1 and I2 given by (2) and (3) within the given dead time. For light load conditions in which there is insufficient inductive stored energy to discharge the capacitive energy of the MOSFETs, the dead time could be raised according to the current in order to realise ZVS [26]. The graph also illustrates that when the voltage transfer ratio deviates from unity for a given value of inductance, the converter switches suffer hard switching. So long as the voltage transfer ratio remains unity, soft switching is achieved across both the primary and secondary legs. The most essential aspect to remember is that the soft switching region is dependent on the leakage inductance value. As the inductance value rises, the soft-switching capability of the converter increases to very low power levels (or light loads), as previously stated.

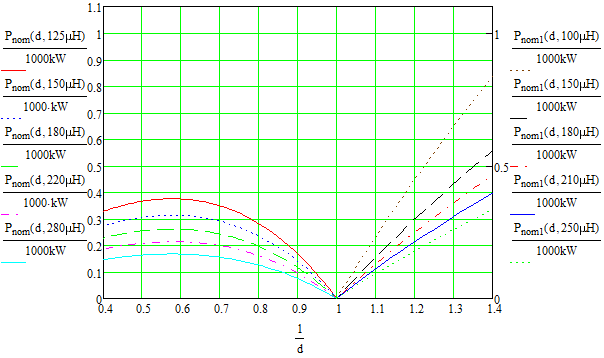


Fig. 39 – ZVS range and the normalised output power against the voltage transfer ratio M from (11).

## Losses of BPSFB converter

In order to compute the secondary RMS currents, the output current ripple is necessary to be defined [27]. It can be considered 20% of the output current, for example. In this case, the current ripple on the output inductor is:

The waveforms of the main currents of the converter are presented on Fig. 40 below.

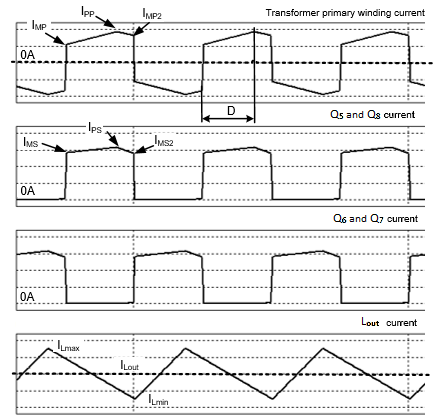


Fig. 40 – Main current of the phase-shift converter.

The secondary RMS currents from Fig. 40:

The diode RMS currents:

where Dmax is the maximum duty cycle. Then, to compute the primary RMS currents, the variation of the current of the magnetising inductance is calculated first:

where η is the minimum full load efficiency.

Finally, the transistor losses can be calculated in the same way as in the case of DAB, using the selected MOSFET’s data sheet or alternatively, reading the gate charge and the output capacitor of the transistor from the data sheet and using this formula [27]:

In (67), Qg and Vg are the total gate charge of the MOSFET and the voltage applied to the gate to activate the MOSFET, from the transistor data sheet. Our Infineon BPSFB converter board used in the experimental prototype achieves a peak efficiency of 98.05% in forward mode and 97.5% in backward mode at nominal conditions and 50% load. Its specific volume occupancy is 0.76L, which corresponds to 4.34kW/L power density at the peak power of 3300W [28]. Since the same board is modified into a DAB converter, it has similar efficiency.

## Impact of SiC semiconductors on system efficiency and power density

There is already well known, that the use of medium frequency transformers (MFT)s alone allow significant power density improvements and weigh reduction, when compared to the traditional traction systems. The first PETT implemented and tested on a real locomotive by ABB obtained 0.5 to 0.75kVA/kg compared to the 0.2-0.35 kVA/kg of conventional traction chains, and they did not even use WBG semiconductors at that time [24]. However, latest results and prototypes found in state of the art literature shows a great increase in power density and efficiency, especially works employing SiC devices.

The new traction systems can be equipped with converter modules using the latest Silicon Carbide (SiC) or other WBG technologies to obtain great performance and power density [18]–[20]. In [21] there is a study included about the benefits of WBG semiconductors in PETTs. The concept of exchanging bulky and heavy line transformers with modular PETTs is already well researched and developed since 85’ [22], however it was always focused on AC electrification systems [23]. The first full-scale PETT tested on a locomotive was presented in [24] and currently a full-scale model is under development, for the first time, for the newly proposed MVDC electrification (the 9kV variant) in [25], as a part of another project, named FUNDRES. In the following a short review on the impact of SiC semiconductors on system efficiency and power density will be presented.

### Power density

The manufacturer of our experimental board, Infineon, presented another bidirectional, 11kW CLLC DC converter with 1700 and 1200V SiC MOSFETs. The converter is only 3.74L and achieves 5.5kW/kg power density [29].

Another work, presented in [30], discusses a the design optimisation of a DAB converter intended for on-board chargers, capable of 3.3kW – same power rate as our BPSFB prototype board. They achieved a final projected power density of 5.44kW/L, which is, as expected, slightly better as of the phase-shift converter’s (however, the full-bridge modules features SiC MOSFETs). The results also demonstrate the ZVS capabilities over the entire charging profile, with 98% peak efficiency. The paper is very detailed on every aspect, including design and experimental results.

In [28] a Half-Bridge cell based Modular Multi-level converter (MMC) for MV Variable Speed Drive (VSD) is used to evaluate and compare the impact of SiC MOSFETs against Si insulated gate bipolar transistors (IGBTs), on the efficiency and power density. Based on analytical methods and simulation of the 7kV DC – 4.16kV AC, 1MVA MVVSD with 1.7kV SiC devices, the following results were obtained: 2.56 times lower switching and conduction losses at low frequency conditions and 4.44 times lower losses on transistors at peak power, using SiC design; smaller heat sink for SiC devices; 1.6 smaller submodule volume; and better output current THD. The value of peak efficiency and power density obtained with SiC was 99.64% and 1.7MVA/m3 respectively for the same switching frequency for both SiC and IGBT. The case study was done on a full-scale experimental prototype.

In [31] a 100kW SiC MOSFET (1200V, 600A) based single cell Switched Tank Converter especially for transportation electrification is presented, including design of components and other devices. The obtained power density of the main circuit is about 42 kW/L and the efficiency is 97.40 – 98.70% depending on the load. Furthermore, the introduction section of the paper offers a good review on the power density improvements obtained in other works, using SiC devices.

Papers [32], [33] present a MW scale hybrid-electric propulsion system for Aircraft applications. The power inverter is based on a 3-level active NPC converter emerging both SiC and Si semiconductors. The DC BUS voltage is 2.4kV and the inverter has a 1.4 kHz output frequency for the high-speed motor drive. The concept presented in this work helps with motor weight reduction and high power density achievements. It was shown that the system can reach 99% efficiency, 18kVA/kg and 10MVA/m3 power density (the full scale prototype, including the power stage, filters, mechanical components and auxiliary power supplies has 125L cabinet volume and weights 70kg, while having 1.3MVA continuous power rating).

Reference [34] describes another bidirectional DC-DC converter, intended for high-power applications. The paper presents an optimized design using high-performance four split-cores and dual-foil winding inductors, validated on an 80kW SiC converter experimentally, obtaining 31.4kW/L and 15.7kW/kg power density with 97% averaged efficiency. The paper also mentions of a goal of the US Department of Energy’s roadmap to achieve 100kW/L power by 2025.

Two other valuable works are presented in [35] and [36], which is a very useful guide for the industry on PETT design and implementation. In [35] technical challenges of the MFT design and trade-offs are discussed. The paper presents a dedicated algorithm for design optimisations – a powerful tool generating feasible MFT designs for the given requirements. It is intended for modular ISOP DC-DC systems. The design variations are also compared take into account weight and volume, maximum achievable efficiency, to identify the design limitations. For the investigated variants of MFT design choices and materials, it was determined that the highest power densities are obtained in the frequency range of around 10 to 20 kHz. The other useful methodology from [36] is an optimization of PETT sizing for a given application. The procedure proposed can maximise the converter’s efficiency under a limited volume. In the paper a 2MW traction converter is considered for the 25kV AC catenary. The whole procedure is illustrated via simulation on a converter featuring 3.3kV SiC semiconductors. As results, 98.9% best efficiency is achieved with 23 modules, 28.6L each.

### Efficiency

Since commercial 3.3 kV SiC MOSFETs are available, different works and papers present case studies and prototypes, offering actual results on efficiency improvement. In [37] three different variants of an insulated DC-DC converter is sized for maximum efficiency under weight and volume constraints. They are sized for a 2MW PETT on the 15kV/16.67Hz railway electrification system, featuring 3.3 kV SiC MOSFETs and 6 kHz MFTs with cast resin insulation and nanocrystalline C-core. The lowest losses were obtained employing full-bridge configuration in primary and secondary sides as well, achieving 99.17% efficiency at nominal power. The authors concluded that due to the use of forced air cooling instead of liquid cooling improves the maintenance of the PETT, compared to traditional line frequency transformer (LFT) based traction systems. The same authors in [38] using the PETT design that achieved the highest efficiency in [37], presented an optimisation of the typical mission profile. As a result of design optimisation of the DC-DC converter a 13% of total energy loss reduction was obtained during a typical journey, in a regional application. The key in achieving that improvement was to target the design optimisation and sizing methodology for the mission profile rather than the operation at nominal power, in this way maximising the efficiency. Energy losses were defined for each phase: acceleration, cruising, coasting, braking and stop.

The IK4- IKERLAN Technological Research Centre in Spain presented a good case study on a first full-SiC DC-DC converter between the catenary side DC link and the energy storage system, in railway application. In [39] due to the different packaging and current rates of SiC devices, the authors present a re-design of the converter, which resulted in 30% total size reduction. The lower switching energy of the new devices allowed such a reduction of power losses, that the switching frequency could be raised more than 10 times. The paper presents a new inductor design as well, employing amorphous magnetic cores that are suitable for high frequency and high current levels. A 73% of size reduction of the inductors was obtained.

Paper [40] offers a comparative performance evaluation of the SiC MOSFET, junction-gate field-effect transistor (JFET) and Si IGBT devices using a DC-DC boost converter. In the analysis the energy losses and switching characteristics were compared at different load currents and switching frequencies. Results demonstrated that the SiC devices outperformed the Si IGBT due to lower switching losses (up to 4 times, depending on the load current) and on-state resistance. The SiC devices also operates at higher frequencies, for example the SiC MOSFET at 20 kHz maintained efficiency above 97% on the whole range of output powers.

Another journal paper, [20], traces the development of high-power SiC and hybrid SiC devices in railway traction systems applications. As a result of static and dynamic testing, higher efficiency, power density and better performance was concluded when compared to Si IGBT modules, especially in higher frequency and temperature conditions. The current challenges of SiC devices and their future potential for the next generation solid state transformers (SSTs) of railway transportation and renewable energy integration are also highlighted.

In [41] a modular high-frequency SiC SST is presented, for MV applications, covering the converter design, its system-level integration, the control architecture and soft-switching analysis. The topology is a bidirectional full-bridge CLLC DC converter. The experimental evaluation results in efficiency exceeding 98.5%, while with line bridges included 98% overall.

Finally, the very recently developed PETT prototype for the French proposed 9kV DC railway electrification system is implemented with 3.3kV SiC MOSFETs at 15kHz switching frequency [42]. At nominal output power, a remarkable 98.93% efficiency of is obtained [25]. Before developing the DC PETT, in [19] the operation in ZVS mode of two SiC MOSFETs with different current ratings were studied, the 1.7kV/1100A and the 3.3kV/750A module. They presented a driver design and a test-bench, which allows the measurement of switching energies. The experimental results validated the capability to operate at ZVS of the gate driver. Based on the estimations and simulation results of the paper, the authors later developed and published last year the 600 kW DC PETT prototype mentioned above, using the 3.3kV SiC modules. It is interesting to mention that they used a resonant DAB topology in ISOP connection, a similar configuration we proposed in D2.1. This also validates our literature research conclusions from 2020.

# Discussions and conclusion

As a result of implementing two slightly different converter topologies as candidates for the PETT modules, the following conclusions were obtained, summarised in Table 3 below:

Table 3 – Comparison of DAB and BPSFB converters.

| DAB converter | BPSFB converter |
| --- | --- |
| *First order system*:  Simpler small signal model and easier to compensate (with a PI) | *Second order system:*  More complex small signal model and regulator design, a PID is necessary |
| Easier component design, leakage inductance can be integrated into the transformer | More complicated design procedure, output inductor can be difficult to design and integrate |
| It can be more compact | It may have higher volume then DAB, because of the output inductor |
| Easier to control the converter in for-ward and backward modes (both can be controlled with the phase shift only) | Forward and backward modes differ, even as small signal models, two different control mode is necessary, one for buck and one for boost mode |
| It can be more efficient at high power rates (no output inductor) | Efficiency may be limited, significant losses on output inductor at high power |
| Presents better cost-benefit ratio | Somewhat higher costs than DAB |
| ZVS can be obtained  on the whole range of power | ZVS cannot be obtained  on the whole range of power |

The two converters being compared, the DAB modules seems to be a simpler and more cost-performance effective solution for the traction system. Its suitability and performance was proved via the full-scale software model on the whole range of possible catenary voltage. The efficiency of full-bridge topologies proposed in D2.1 was validated through both converter topologies and the short literature review about the power density and efficiency as well.

This report included a detailed mathematical model including some key design considerations and losses evaluation guide. Moreover, the compensator design equations were also derived for both PI and PID controllers, using the frequency domain method.

As a result of the performance evaluation of the DC PETT, it can be concluded that a power density of tens of MW/m3 is possible to achieve employing SiC devices in modular MFT systems with switching frequency between 10-20 kHz.

MVDC-ERS presents a concept of a new DC railway electrification system, based on the new technology that makes possible its implementation. Such a novel system opens new opportunities and functionalities of an interoperable smart DC grid. At the same time, the new system will combine the advantages of various new technology and the advantages of current railway electrification systems, as presented in D2.1 and D1.1. The on-board PETTs were necessary to be redefined and designed for the new system and its needs. Such a full-scale system was designed in MVDC-ERS as an example and presented here, using the best possible PETT configuration found suitable as a result of the literature research from D2.1.

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